Notice of Allowability	Application No.	Applicant(s)	
	09/920,222	DAVIES, ROBERT B.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/27/05*.

2. ☒ The allowed claim(s) is/are *1,2,4-7,37 and 39-48*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 08/01
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EUGENE LEE
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DETAILED ACTION

Examiner's Amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Claims 8 thru 27, and 34 thru 36, previously withdrawn from consideration for being drawn towards a non-elected invention, have been cancelled.

Allowable Subject Matter

2. Claims 1, 2, 4 thru 7, 37, and 39 thru 48 are allowed.

3. The following is an examiner's statement of reasons for allowance: The references of record, either singularly or in combination, do not teach or suggest at least an integrated circuit, comprising: a low resistivity semiconductor substrate having a dielectric region formed therein, a trench; an adjacent cavity; an electroplated conductive material disposed within the trench to produce an inductance; a bottom surface of the semiconductor substrate defining a first recessed region underlying the dielectric region (claims 1, 2, and 4-7).

Regarding claims 37, 41, and 42, the references of record, either singularly or in combination, do not teach or suggest at least an integrated circuit comprising: a low resistivity, semiconductor substrate including a dielectric region; a trench formed in the dielectric region; high conductivity electroplated material in the trench and defining at least a portion of a passive

electronic component, wherein the low dielectric constant material includes dielectric material defining an array of cavities therein, the dielectric material having a first dielectric constant and the cavities providing a second dielectric constant lower than the first dielectric constant to form an effective dielectric constant lower than the first dielectric constant.

Regarding claims 39, and 40, the references of record, either singularly or in combination, do not teach or suggest at least an integrated circuit comprising: a low resistivity, semiconductor substrate including a dielectric region; a trench formed in the dielectric region and including side-walls defined by low dielectric constant material; high conductivity electroplated material in the trench and defining at least a portion of a passive electronic component; and wherein the low dielectric constant material includes dielectric material defining an array of cavities therein, the dielectric material having a first dielectric constant and the cavities providing a second dielectric constant lower than the first dielectric constant to form an effective dielectric constant lower than the first dielectric constant.

Regarding claims 43, and 44, the references of record, either singularly or in combination, do not teach or suggest at least an integrated circuit comprising: a low resistivity, semiconductor substrate including a dielectric region; a trench formed in the dielectric region; high conductivity electroplated material in the trench and defining at least a portion of a passive electronic component; and further including a cavity at least partially defined by the substrate in the dielectric region and in communication with a lower portion of the high conductivity, electroplated material in the trench.

Regarding claims 45-48, the references of record, either singularly or in combination, do not teach or suggest at least an integrated circuit comprising: a low resistivity, semiconductor

substrate including a dielectric region; an elongated trench formed in the dielectric region; high conductivity material in the trench and defining at least a portion of an inductive component; and a sealed cavity at least partially defined by the substrate in the dielectric region and in communication with a lower portion of the high conductivity material in the trench.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
March 14, 2006

AU 2815